

# Output Waveform Evaluation of Basic Pass Transistor Structure\*

S. Nikolaidis<sup>1</sup>, H. Pournara<sup>1</sup>, and A. Chatzigeorgiou<sup>2</sup>

<sup>1</sup> Department of Physics, Aristotle University of Thessaloniki

<sup>2</sup> Department of Applied Informatics, University of Macedonia  
54006 Thessaloniki, Greece

hpour@skiathos.physics.auth.gr

**Abstract.** Pass transistor logic is a promising alternative to conventional CMOS logic for low-power high-performance applications due to the decreased node capacitance and reduced transistor count it offers. However, the lack of supporting design automation tools has hindered the widespread application of pass transistors. In this paper, a simple and robust modeling technique for the timing analysis of the basic pass transistor structure is presented. The proposed methodology is based on the actual phenomena that govern the operation of the pass transistor and enables fast timing simulation of circuits that employ pass transistors as controlled switches without significant loss of accuracy, compared to SPICE simulation.

## 1 Introduction

Pass transistor logic is being increasingly used in digital circuits due to the advantages that it offers compared to other logic families for a class of logic functions. The use of pass transistors as transfer gates is a promising approach in reducing the physical capacitance being switched in a circuit and in this way offers significant power savings and speed improvement over conventional CMOS implementation. Pass transistor logic styles are very efficient in terms of transistor count for designs that employ the XOR and MUX operation [1] and as a result very compact and fast full adder implementations have been proposed [2], [3], [4].

Although pass transistor logic is attractive for low-power high-performance circuit design it is rarely the logic style of choice for actual designs. The main reason behind this limited application of pass transistor logic, are not the inherent problems of pass transistors such as the threshold drop or the need for level restoring devices, as it is widely believed. Rather, it is the lack of appropriate design automation tools that can support pass transistor implementation during all phases of the system design hierarchy. One aspect of this scarcity in tools can be identified in the limited number of fast timing analysis techniques for pass transistors.

Over the last decade modeling techniques for static CMOS gates, with emphasis on the inverter, have matured to offer significant speed improvement over SPICE-

\* This work was supported by AMDREL project, IST-2001-34379, funded by the European Union"

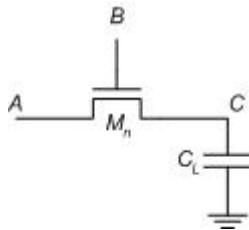
based simulators and a level of accuracy, which is acceptable for most applications [5]-[10]. However, the difficulty in solving the circuit differential equations for pass-transistor structures has resulted in a limited number of modeling techniques for such circuits. Among them is a delay-macromodeling technique for transmission gates [11], a simplified analysis of a single pass transistor driven by a step input [12] and a semi-analytical approach in modeling CPL gates by partitioning into smaller sub-circuits [13].

In this paper, the analysis of the basic pass transistor structure, namely an nMOS pass-transistor with one terminal driven by the output of a previous logic stage and the other connected to a single capacitance, will be presented. The operation of this circuit will be analyzed for a constant driving signal and a rising ramp applied at the gate of the pass transistor. This scheme, resembles an often use of pass-transistors in actual designs as a controlled switch which transfers or not the input signal, depending on a control signal, which usually arrives later.

The rest of this paper is organized as follows: Section 2 describes the mode of operation of the pass-transistor and the formulation of the circuit differential equation to be solved. In section 3 the evaluation of the output waveform based on the proposed current model is presented, while simulation results for the proposed method are compared with SPICE in section 4. Finally, we conclude in section 5.

## 2 Analysis of Operation

The operation of the pass transistor will be studied using the structure shown in Fig. 1. The output capacitance  $C_L$  models the gate capacitance of the next level logic gates. Node A is set at logic "0" or "1" and an input ramp is applied to the gate of the pass transistor, node B. Consequently, the pass transistor will either discharge or charge the output capacitance towards logic "0" or "1", respectively.



**Fig. 1.** Basic pass transistor structure

Let us consider first the case when the output capacitance is initially charged while the node A is set to logic low and a ramp input is applied to node B. In this case the output capacitance is discharged with a current flowing from node C to node A so that node A is the source node of the transistor. The operating condition of the transistor corresponds to that of the nMOS transistor of an inverter when a rising ramp is applied to its gate and the contribution of the short-circuiting transistor is ignored. As the input voltage rises, the transistor starts operating in saturation and after some time it moves to the linear region. The differential equations describing the circuit operation at both regions can be solved analytically and the output waveform

can be calculated as a function of time. Since such an analysis is well known and uncomplicated it isn't further discussed in this work.

Different operating conditions arise in case the output capacitance is being charged through the pass transistor. The output capacitance is considered initially discharged and node A is set at logic "high" ( $V_{DD}$ ). The charging current flows through the transistor from node A to node C and thus node C is the source of the transistor. According to the conventional Shockley model [14], since  $V_{DS} \geq V_{GS} \forall t$  the transistor operates always in saturation.

To describe the transistor current, the alpha-power law model, proposed in [5], which takes into account the carrier velocity saturation effect of short-channel devices, is used. According to this model, the transistor current expression in saturation is given by:

$$I_{sat} = k_s (V_{GS} - V_{TN})^\alpha \quad (1)$$

where  $k_s$  is the transconductance of the transistor in saturation and  $\alpha$  is the velocity saturation index, which both are determined by measurements on the  $I$ - $V$  characteristics [5].  $V_{TN}$  is the threshold voltage of the nMOS transistor, which is expressed by its first order Taylor series approximation around  $V_{out} = (V_{DD} - V_{TO})/2$  as:

$$V_{TN} = d_1 \cdot V_{out} + d_2 \quad (2)$$

( $V_{TO}$  is the zero-bias threshold voltage [14]).

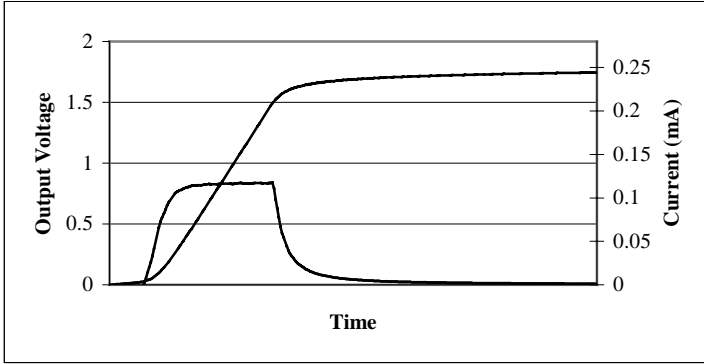
The fact that the same node (C) serves as output node of the circuit and as source node of the pass transistor makes the analysis of the transistor operation cumbersome, since the differential equation that describes the charging of the output capacitance has the form:

$$C_L \frac{dV_{out}}{dt} = k_s (V_{in} - V_{out} - V_{TN})^\alpha \quad (3)$$

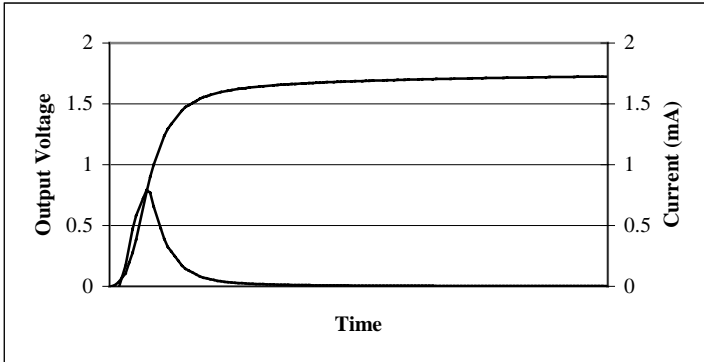
which cannot be solved analytically, since  $\alpha$  has a value different than one, even for deep submicron technologies. However, making some reasonable approximations for the transistor current waveform, the output voltage can be modeled with sufficient accuracy.

In order to solve the circuit differential equation two cases for the input ramp are distinguished, namely fast and slow input ramps. In Figs. 2, 3 the model for the current waveform for each case is shown (with respect to the output voltage waveform). For slow input ramps (Fig. 2) the current waveform presents a plateau region where the value of the current remains constant. When a plateau region is not present on the current waveform (Fig. 3) the input ramp should be considered fast. The appearance of the plateau region depends on the slope of the input ramp and the circuit inertia, i.e. the transistor width and the load capacitance. The transistor starts conducting with its current increasing exponentially, according to equation (1). Following the current, the output voltage increases exponentially until time  $t_p$  when the rate of  $V_{out} - V_{TN}$  increase, equals the rate of input increase. Then the output voltage increases linearly with a constant rate since the transistor current has a constant plateau value. This region of operation continues until the end of the input transition at time point  $\tau$  where the input voltage reaches its final value and the current starts to decrease since the output voltage increases ( $V_{GS}$  decreases). Although the

starting point of the plateau,  $t_p$ , is not always distinct, because of a smooth transition of the current in this region, the plateau region is easily identified. However, if the slope of the input ramp or the circuit inertia is sufficiently high, as in the case of a large output capacitance, the rate of increase of  $V_{out} - V_{TN}$  may not reach the input slope until the end of the input ramp and the current will start decreasing without the appearance of the plateau region (fast input case).



**Fig. 2.** Output voltage and current waveforms for a slow input case ( $\tau=0.5\text{ns}$ ,  $W=1.8\mu\text{m}$ ,  $C_L=30\text{fF}$ ),  $V_{DD}=2.5\text{V}$



**Fig. 3.** Output voltage and current waveforms for a fast input case ( $\tau=0.05\text{ns}$ ,  $W=1.8\mu\text{m}$ ,  $C_L=30\text{fF}$ ),  $V_{DD}=2.5\text{V}$

### 3 Output Waveform Evaluation

#### 3.1 Slow Input Ramps

##### *Region 1* ( $1.3t_n \leq t < t_p$ )

According to simulation results it can be safely assumed that the current in this region varies linearly with respect to time and consequently it can be approximated as:

$$I = \gamma \cdot (t - 1.3t_n) \quad (4)$$

where  $t_n$  is the time point where the input ramp reaches the threshold voltage of the nMOS transistor ( $t_n = V_{TO} \cdot \tau / V_{DD}$ ). In order to calculate the output waveform with accuracy, two approximations on the starting point of the current and output waveform are being made: a) that the current and output voltage waveform remains equal to zero up to  $t=1.3t_n$  as it can be seen from the region boundary and b) that the output voltage can be considered equal to zero up to time point  $\tau/4$  ( $V_{out}(\tau/4) = V_0 = 0$ ), fact that it can be safely assumed according to simulation results. By equating the current expression in saturation with the approximated current form in (4) at time point  $t = \tau/4$  the coefficient  $\gamma$  can be obtained:

$$k_s \left[ V_{in} \left( \frac{\tau}{4} \right) - V_o - V_{TN} \left( \frac{\tau}{4} \right) \right]^\alpha = \gamma \cdot \left( \frac{\tau}{4} - 1.3t_n \right) \quad (5)$$

To increase the accuracy in modeling the current in this region, the value of the transconductance parameter  $k_s$  and that of the velocity saturation index  $\alpha$  are calculated on the  $I$ - $V$  characteristics of the nMOS transistor for very low  $V_{GS}$  values and high  $V_{DS}$  values, in order to capture the actual operating conditions of the pass transistor in this region. It should be noted, that according to extensive simulation results, these parameters for the alpha-power law model rely heavily on the region of the  $I$ - $V$  characteristics on which they are calculated rather than being constant as implied by [5]. In Table I the values of  $\alpha$  and  $k_s$  as they are extracted for various combinations of  $V_{GS}$  and  $V_{DS}$  and for the used technology, are given.

**Table 1.** Values of  $\alpha$  and  $k_s$  for various  $V_{GS}$  and  $V_{DS}$  ( $W=1,8\mu\text{m}$ )

$V_{GS}$ (V)	$V_{DS}$ (V)	$\alpha$	$k_s$ (mA/V)	$V_{GS}$ (V)	$V_{DS}$ (V)	$\alpha$	$k_s$ (mA/V)
2.4	2.4	1.12	0.74	0.7	2.45	2.02	1.14
2	2	1.12	0.72	0.6	2	2.84	2.41
1.5	2	1.23	0.71	0.7	2	2.17	1.17
1.5	1.5	1.26	0.67	0.6	2.45	2.63	2.20
1	2	1.47	0.72	0.5	2.45	2.93	3.36

The shaded values were used in eq. (5) for the analysis in this region, since, as it was observed by simulation, they are close to the real values of  $V_{GS}$  and  $V_{DS}$ . The output waveform expression in this region is calculated by solving the circuit differential equation:

$$C_L \frac{dV_{out}}{dt} = \gamma \cdot (t - 1.3t_n) \quad (6)$$

with initial condition  $V_{out}[1.3t_n] = 0$ .

### Region 2 ( $t_p \leq t < \tau$ )

For slow input ramps there will be a time point ( $t_p$ ) where the output voltage will increase at a rate that will keep the current at a constant value. From this point and

until the input reaches its final value this constant current results in a "plateau" for the current waveform (Fig. 2). The time point when this plateau state begins is calculated by equating the slope of the input voltage to the slope of the output, considering the effect of the varying threshold voltage:

$$\left. \frac{d(V_{out} + V_{TN})}{dt} \right|_{t=t_p} = \left. \frac{dV_{in}}{dt} \right|_{t=t_p} \tag{7}$$

The current value during the plateau is simply given by:

$$I_{plateau} = \gamma(t_p - 1.3t_n) \tag{8}$$

The output voltage is a first order polynomial expression derived from the following differential equation:

$$C_L \frac{dV_{out}}{dt} = I_{plateau} \Rightarrow V_{out}(t) = I_{plateau} \cdot (t - t_p) / C_L + V[t_p] \tag{9}$$

**Region 3 ( $t \geq \tau$ )**

In this region the input voltage is equal to  $V_{DD}$  while the current decreases exponentially with respect to time. We assume that the current is described by an expression of the form:

$$I(t) = I_{plateau} \cdot e^{-\beta(t-\tau)} \tag{10}$$

The output voltage is calculated by solving the circuit differential equation with initial condition the value of the output voltage at time point  $\tau$ , which is known from the previous region.

In order to calculate the value of  $\beta$  which is unknown in eq. (10), the charge that is being stored at the output capacitance during region 3 is calculated:

$$Q = \int_{\tau}^{\infty} I_{plateau} \cdot e^{-\beta(t-\tau)} dt = I_{plateau} / \beta \tag{11}$$

This amount of charge can be expressed as the difference between the final charge stored in the output load and that which is stored at time  $\tau$ .

$$Q = C_L \cdot (V_{out}[\infty] - V_{out}[\tau]) \tag{12}$$

where the output voltage after infinite time is given by  $V_{out}[\infty] = \frac{V_{DD} - d_2}{1 + d_1}$  due to threshold voltage drop across the pass transistor. By equating eq. (11) and (12) the value of  $\beta$  is obtained.

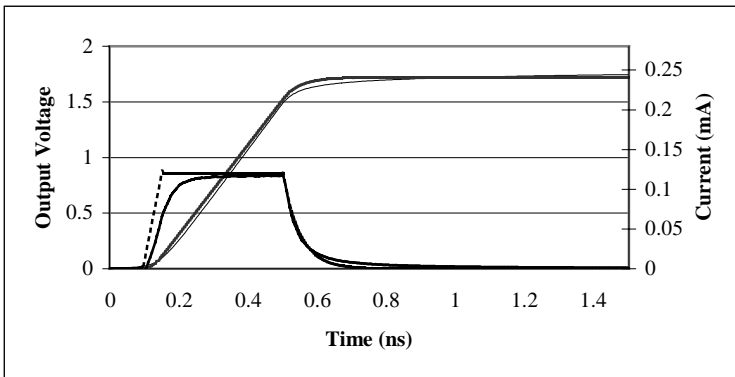
**3.2 Fast Input Ramps**

In this case only two regions of operation exist since the input voltage reaches  $V_{DD}$  before the current enters the plateau state. As a result, the boundary between the two regions is time point  $\tau$  and the output voltage at each region is calculated exactly as for regions 1 and 3 for slow input ramps.

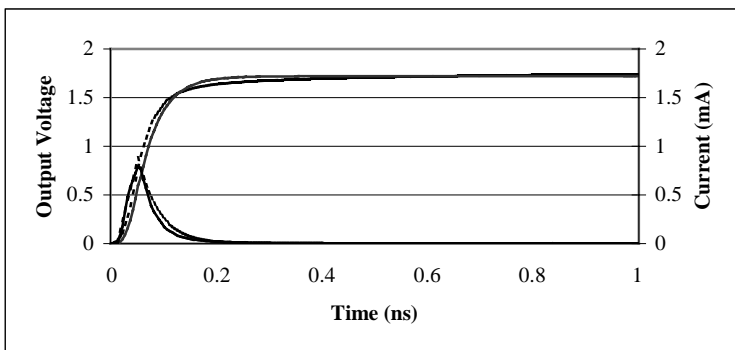
To determine whether an input corresponds to the fast or slow case, after the calculation of the output voltage expression in the first region, equation (7) is being solved. In case the resulting  $t_p$  time point is smaller than the transition time  $\tau$ , the input is considered slow, otherwise the solution for the fast input case is being followed.

## 4 Results

The proposed methodology has been validated by comparisons with HSPICE simulation results for a TSMC 0.18  $\mu\text{m}$  technology. To prove the efficiency in modeling the pass transistor current, output voltage and current waveforms generated by the proposed method are compared with SPICE simulation results in Figs 4, 5, for a slow and a fast input case, respectively. The presence of the plateau for the slow input case and the validity of the proposed current model are obvious from these figures.

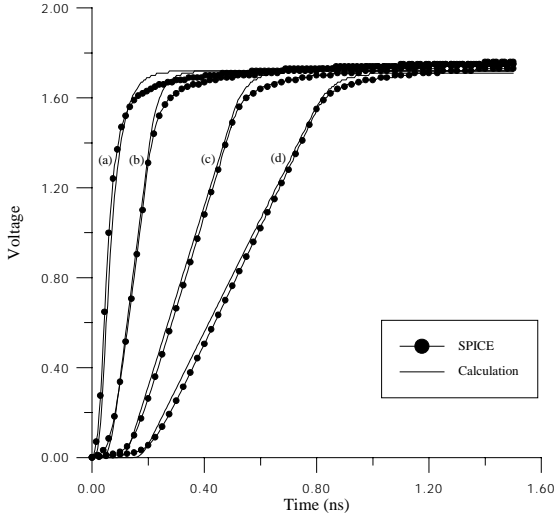


**Fig. 4.** Output voltage and current waveform comparison between SPICE (solid lines) and calculated results (dashed lines), for a slow input case ( $\tau=0.5\text{ns}$ ,  $W=1.8\mu\text{m}$ ,  $C_L=30\text{fF}$ ).

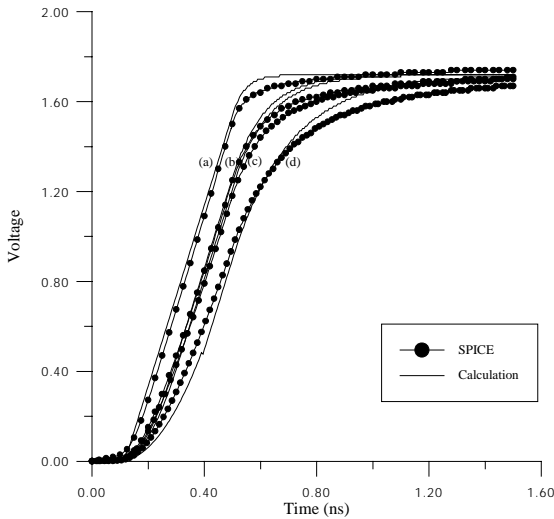


**Fig. 5.** Output voltage and current waveform comparison between SPICE (solid lines) and calculated results (dashed lines), for a fast input case ( $\tau=0.05\text{ns}$ ,  $W=1.8\mu\text{m}$ ,  $C_L=30\text{fF}$ ).

To illustrate the applicability of the proposed method, comparisons with SPICE results have been performed for a number of input transition times and circuit configurations (pass transistor width and output capacitance). Figs. 6, 7 and 8 show output waveform results for varying input transition times, transistor widths and output capacitances, respectively.

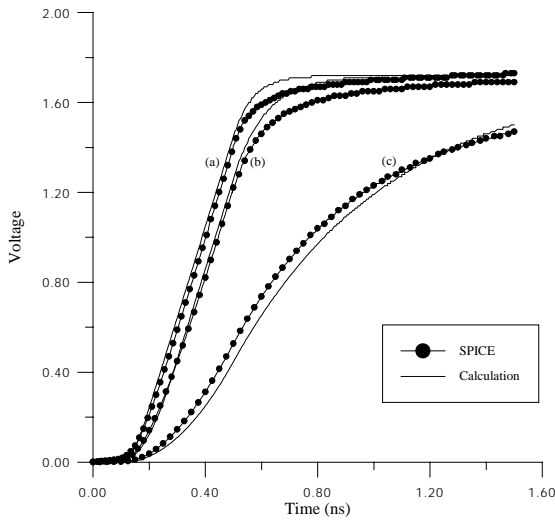


**Fig. 6.** Output waveform comparison between SPICE and calculation for  $W=1.8 \mu\text{m}$ ,  $C_L=30\text{fF}$  and varying input transition times (a)  $\tau=0.05\text{ns}$ , (b)  $\tau=0.2\text{ns}$ , (c)  $\tau=0.5\text{ns}$ , (d)  $\tau=0.8\text{ns}$



**Fig. 7.** Output waveform comparison between SPICE and calculation for  $\tau=0.5 \text{ ns}$ ,  $C_L=50\text{fF}$  and varying transistor widths (a)  $W=3.6 \mu\text{m}$ , (b)  $W=0.9 \mu\text{m}$ , (c)  $W=0.72 \mu\text{m}$ , (d)  $W=0.36 \mu\text{m}$





**Fig. 8.** Output waveform comparison between SPICE and calculation for  $\tau=0.5$  ns,  $W=1.8$   $\mu\text{m}$  and varying output capacitance (a)  $C_L=50$  fF (b)  $C_L=100$  fF, (c)  $C_L=500$  fF

Defining propagation delay as the time from the half- $V_{DD}$  point of the input waveform to the half- $V_{DD}$  point of the output, propagation delay results have been obtained and compared with SPICE simulations (Table II). The error between SPICE and the proposed method, in spite of the approximations used in the current model, remains for most of the cases below 7%.

**Table 2.** Propagation delay comparison between SPICE and the proposed method

	<i>Prop. Delay (SPICE)</i>	<i>Prop. Delay (method)</i>	<i>Error</i>
$C_L = 30$ fF, $W=1.8\mu\text{m}$	(ps)	(ps)	(%)
$\tau(\text{ns})$			
0.8	267	275	3.0
0.5	192	182.5	4.9
0.2	95	90	5.3
0.05	51	60	17.6
$C_L = 50$ fF, $\tau=0.5$ ns			
$W$ ( $\mu\text{m}$ )			
3.6	190	177.5	6.6
0.9	250	247.5	1.0
0.72	269	260	3.3
0.36	362	365	0.8
$\tau = 0.5$ ns, $W=1.8$ $\mu\text{m}$			
$C_L$ (fF)			
500	770	810	5.2
100	258	247.5	4.1
50	213	200	6.1
30	192	182.5	4.9

## 5 Conclusions

Pass transistor logic is becoming increasingly important for the design of low-power high-performance digital circuits due to the smaller node capacitances and reduced transistor count it offers compared to conventional CMOS logic. However, the acceptance and application of pass transistor logic depends on the availability of supporting automation tools. One aspect of this issue concerns timing simulators that can analyze the performance of large circuits at a speed, significantly faster than that of SPICE based tools. In this paper, a simple and robust modeling technique for the basic pass transistor structure is presented, which offers the possibility of fast timing analysis for circuits that employ pass transistors as controlled switches. The proposed methodology takes advantage of the physical mechanisms in the pass transistor operation. The obtained accuracy compared to SPICE simulation results is sufficient for a wide range of input and circuit parameters.

## References

1. Zimmermann R. and Fichtner W.: Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic, *IEEE J. Solid-State Circuits*, Vol. 32, (1997), 1079-1090
2. Suzuki M., Ohkubo N., Shinbo T., Yamanaka T., Shimizu A., Sasaki K. and Nakagome Y.: A 1.5-ns 32-b CMOS ALU in Double Pass-Transistor Logic, *IEEE J. Solid-State Circuits*, vol. 28, (1993), 1145-1150
3. Abu-Khater I.S., Bellaouar A., Elmasry M. I.: Circuit Techniques for CMOS Low-Power High-Performance Multipliers, *IEEE J. Solid-State Circuits*, vol. 31, (1996), 1535-1546
4. Yano K., Sasaki Y., Rikino K. and Seki K.: Top-Down Pass-Transistor Logic Design, *IEEE J. Solid-State Circuits*, vol. 31, (1996) 792-803
5. Sakurai T., Newton A.R.: Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas, *IEEE J. Solid-State Circuits*, Vol. 25, (1990), 584-594
6. Juan-Chico J., Bellido M. J., Acosta A. J., Barriga A., Valencia M.: Delay degradation effect in submicronic CMOS inverters, *Proc. of 7th Int. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, (1997), 215-224
7. L. Bisdounis, S. Nikolaidis, O. Koufopavlou, «Analytical Transient Response and Propagation Delay Evaluation of the CMOS Inverter for Short-channel Devices», *IEEE Journal of Solid-State Circuits*, Vol. 33, No 2, pp. 302-306, Feb. 1998.
8. Daga J. M. and Auvergne D.: A Comprehensive Delay Macro Modeling for Submicrometer CMOS Logics, *IEEE J. Solid-State Circuits*, Vol. (34), (1999), 42-55
9. Chatzigeorgiou A., Nikolaidis S. and Tsoukalas I.: A Modeling Technique for CMOS Gates, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, (1999), 557-575
10. Rossello J. L. and Segura J.: Charge-Based Analytical Model for the Evaluation of Power Consumption in Submicron CMOS Buffers, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 21, (2002), 433-448
11. Vemuru S. R.: Delay-Macromodelling of CMOS Transmission-Gate-Based-Circuits, *International Journal of Modelling and Simulation*, vol. 15, (1995), 90-97
12. Kang S. M. and Leblebici Y.: *CMOS Digital Integrated Circuits, Analysis and Design*, McGraw Hill, New York (1996)
13. Chatzigeorgiou A., Nikolaidis S. and I. Tsoukalas I.: Timing Analysis of Pass Transistor and CPL Gates, *Proc. of 9th Int. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, (1999), 367-376
14. Weste N. H. E. and Eshraghian K., *Principles of CMOS VLSI Design*, Addison Wesley, Reading (1994)